REMARKS

Claims 1-20 are pending in the application.

Claims 4-20 are withdrawn from consideration.

Claims 1-3 are rejected under 35 U.S.C. 103(a).

Claims 1 and 2 are currently amended.

New claims 21-24 are added.

No new matter is added. For example, claim 2 now recites "charge storage dielectric layer" instead of "silicon nitride layer." Support can be found in the specification at page 10, lines 14-15. It is well known in the art that the silicon nitride layer functions as a charge dielectric layer in a SONOS device. The term "silicon nitride layer" is merely replaced with the term "charge storage dielectric layer" to make its implicit function explicit. Therefore, no new matter is presented with this amendment. With respect to new claim 24, support for the limitations can be found in FIG. 10 and the accompanying text.

Claims 1-3 and 21-24 remain in the case for consideration.

Applicant requests reconsideration and allowance of the claims in light of the above amendments and following remarks.

Claim Rejections – 35 U.S.C. § 103

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art ("AAPA") in view of Chang (Chang, et al.; 6,004,841).

Applicants respectfully traverse the rejections.

With respect to independent claim 1, the claim recites a gate electrode having a polysilicon layer and a silicide layer while it also recites, "a resistor pattern having a *single-layer* polysilicon layer and *substantially the entire resistor pattern does not have a silicide layer disposed thereon.*" Support for this is found at, for example, page 5, lines 3-6 and page 6, lines 1-14 and in FIGS. 9-10.

Therefore, in the claimed invention, the electrode structure of the resistor pattern is quite different from that of the gate electrode. In particular, the silicide layer 112b is removed to expose the resistor pattern 108. This is because it is not desirable for the resistor pattern to have a silicide layer (having a high conductivity) disposed thereon as the resulting structure would not successfully function as a resistor.

In contrast, Chang is rather directed to a single fabrication process to form both a capacitor structure, and MOSFET device rather than to a resistor pattern. See abstract of

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Chang. Moreover, in Chang, the capacitor electrode and the gate electrode each have the *same* electrode structure. In particular, in Chang, the polysilicon layer 8 is deposited and patterned to form both the capacitor bottom electrode and the gate electrode as shown in FIGS. 2 and 3.

To teach or disclose the above-recited feature of the claimed invention, Chang should disclose the gate electrode comprising a polysilicon layer and a silicide layer while disclosing a capacitor bottom electrode structure that does *not* have a silicide layer on substantially the entire polysilicon layer. However, Chang does not teach these of the claimed invention and merely teaches the gate electrode and the capacitor bottom electrode each formed of a single layer polysilicon having substantially the same electrode structure. Further, in Chang, if the silicide layer is formed in the gate electrode, it is also desirable to have a silicide layer on the polysilicon in its capacitor lower electrode structure because the silicide layer helps to reduce a decrease in capacitance due to poly depletion in the capacitor structure as is well known to one skilled in the art. If the silicide layer is removed from the capacitor lower electrode structure to reach the claimed invention, it would degrade the characteristics of the capacitor such as access speed and a capacitance. Further, it also requires unnecessary processing steps with additional manufacturing costs. Therefore, Chang rather teaches away from the claimed invention.

For these reasons, in Chang, there is no motivation or suggestion to remove the silicide layer from the polysilicon layer 8.

Further, claim 1 additionally recites "*the interlayer dielectric layer contacts a portion of the resistor spacer.*" Support for the limitation can be found in the specification, for example, page 5, lines 15-16. One skilled in the art will appreciate that this feature of the claimed invention can be fabricated using the etch selectivity between the silicide layer and the resistor spacer without using a photolithography process. Therefore, applicant respectfully submits that the detailed description regarding how this feature can be fabricated is not required as it is readily apparent to one skilled in the art.

In contrast, in Chang, the spacer does not contact the interlayer dielectric layer 17 as the silicon nitride layer 14 is disposed between the interlayer dielectric layer 17 and the spacers. See FIG. 10 of Chang and compare with FIG. 10 of the present application.

Accordingly, applicant respectfully submits that the cited references, either alone or in combination, do not teach or disclose all of the limitations of claim 1 and, further, there is no motivation or suggestion to combine AAPA with Chang. Thus, the rejection does not present

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prima facie case of obviousness and claim 1 is believed to be allowable over the cited combination and allowance is respectfully requested.

Claims 2-3 and 21-23 depend from claim 1 and inherently include all of the limitations of the base claim. As discussed above, the prior art does not teach the limitations of the base claim much less the further embodiments of the dependent claims. Therefore, claims 2-3 are allowable for their dependency and their own merits. Allowance of these claims is requested.

New Claim

With respect to new claim 24, none of the cited references teach or disclose, "the interlayer dielectric layer contacts a portion of the vertical inner sidewall of the resistor insulating spacers" in addition to the other limitations. Thus, claim 24 is allowable.

In conclusion

For the foregoing reasons, reconsideration and allowance of claims 1-3 and 21-24 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,
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I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number (571) 273-8300 on March 1, 2006.

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